

REMARKS

Claims 1-17, 30-38 were rejected under 35 U.S.C. 102(b) over Yaegashi, U.S. patent no. 6,265,739. The Advisory Action dated April 11, 2005 states:

Applicant contends that Yaegashi's layers (106, 107) formed to provide the floating and control gates are not formed after the layer (106) formed to provide the select transistor gate and the Vpp-Tr gate ... Examiner respectfully disagrees. **Applicant's claimed invention does not explicitly specify that the floating gate and the control gate formed after the first layer formed to provide the select gate...**

Claim 1 is amended to recite that the floating and control gates are **provided entirely** by the one or more second layers formed **after forming the first layer** formed to provide the select gate. Claim 1 also recites, for clarity, that the floating and control gates comprise no portion of the first layer. The rejection is therefore believed to be overcome.

The remaining claims depend from Claim 1. Also, Claim 7 is believed to be allowable for the reasons given in Applicant's AMENDMENT filed October 21, 2004, page 6, last paragraph, and page 7, first paragraph. Claims 32-33 are believed to be allowable for the reasons given in Applicant's REPLY TO FINAL OFFICE ACTION dated March 21, 2005, on page 3.

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 2, 2005.

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Respectfully submitted,

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